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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,427	08/26/2003	Hitoshi Saito	030974	2799

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/647,427	SAITO, HITOSHI	
	Examin r	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this c mmunication appears on the c ver sheet with the c rresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *1-3 and 26-28* is/are withdrawn from consideration.

5)☒ Claim(s) *13-22* is/are allowed.

6)☐ Claim(s) *4-9 and 23-25* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the Election filed May 24, 2004.

Election/Restrictions

Applicant's election of claims 4-25 without traverse in the paper filed May 24, 2004 is acknowledged.

Claims 1-3 and 26-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the paper filed May 24, 2004.

Claim Objections

Claim 10 is objected to because of the following informalities: In line 8, "lager" should be changed to "larger". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,518,146) in view of the admitted prior art.

Regarding claim 4, Singh discloses forming a plurality of first trenches (16) in a first region (15) of a semiconductor substrate (12), forming a plurality of second trenches (14) in a

second region (13) of the substrate, increasing the curvature of a top edge portion of the second trench, filling the first and second trenches with an insulating material (38), and forming a first element in the first region and a second element in the second region (Fig. 1-5; col. 1, ln. 59 – col. 3, ln. 33). Singh discloses that the first element is a logic (peripheral) region transistor and the second element is a non-volatile memory transistor (Abstract). Singh does not specifically disclose that the non-volatile memory transistor in the memory cell region is a high-voltage device, nor that the logic (peripheral) region transistor is a lower-voltage device. The admitted prior art discloses that in the conventional circuit having a memory cell portion and a logic (peripheral) portion on the same wafer, the memory cell portion is typically made up of high-voltage transistors while the logic portion is typically made up of lower-voltage transistors (pg. 6, ln. 5-8). At the time of the invention, it would have been obvious to one of ordinary skill in the art to have the non-volatile memory transistors in the memory portion of the circuit of Singh be high-voltage devices, while the transistors in the logic (peripheral) portion of the circuit be lower-voltage devices because, as is taught by the admitted prior art, this is the conventional way in which to form this type of a integrated circuit.

Regarding claim 5, Singh discloses that the second element is a memory cell of a non-volatile memory and Singh discloses that the first element is a transistor, but Singh does not specifically state that the first element transistor is a MOS transistor. The admitted prior art discloses that the conventional transistor in the logic (peripheral) portion of this type of circuit is a MOS transistor (pg. 4, ln. 5-22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the logic (peripheral) transistor of Singh such that it is a

MOS transistor because, as is taught by the admitted prior art, a MOS transistor is conventionally formed in the logic region of this type of integrated circuit.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,518,146) in view of Ishitsuka et al. (US 6,403,446).

Regarding claim 6, Singh discloses forming a first insulating film (20) in first and second regions of a semiconductor substrate (12), forming on the first insulating film a second insulating film (18) made of a material different from the first insulating film, patterning the second insulating film, etching the first insulating film and the substrate by using the second insulating film as a mask, forming a first trench (16) in first regions of the substrate and forming a second trench (14) in the second region of the substrate, oxidizing inner surfaces of the first and second trenches, and forming a first element-isolating film and a second element-isolating film by filling the first and second trenches with an insulating material (38), and removing the second insulating film (Fig. 1-5; col. 1, ln. 59 – col. 3, ln. 33). Singh does not disclose side-etching only the first insulating film of the second region. Like Singh, Ishitsuka discloses forming a shallow trench isolation structure for an integrated circuit. Ishitsuka teaches that it is beneficial to side-etch the first insulating film surrounding the trench in order to form rounded upper edges of the trench (col. 5, ln. 39 – col. 6, ln. 31). When side-etching of the first insulating film is not carried out, the result is that the insulating film becomes compressed during the oxidation of the trench surface. This causes the upper edges of the trench to form acute angles which negatively impacts the function of the isolation trench. At the time of the invention, it would have been obvious to one of ordinary skill in the art to side-etch the first insulating film of Singh before oxidizing the second trench because Singh teaches that this trench should be formed with rounded edges and

Ishitsuka teaches that by side-etching the insulating film, rounded upper trench edges can be more reliably formed.

Regarding claim 7, Singh discloses that the first insulating film is a pad oxide film and the second insulating film is a nitride film. But Singh does not specifically disclose that the first insulating film is a silicon oxide film nor that the second insulating film is a silicon nitride film. Ishitsuka discloses that successful shallow trench isolation can be performed by using a pad silicon oxide film (formed by oxidizing the semiconductor substrate surface) with a film of silicon nitride on top (col. 3, ln. 49-62). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the pad oxide of Singh of silicon oxide and the nitride film of Singh of silicon nitride because Ishitsuka teaches that these materials may successfully be used to accomplish the formation of a shallow trench isolation element.

Regarding claim 8, Singh does not disclose any process steps after removal of the second insulating film. Ishitsuka discloses that a semiconductor device can be formed by removing the second insulating film, then removing the first insulating film and forming a third insulating film between the first trenches in the first region and forming a fourth insulating film between the second trenches in the second region (col. 4, ln. 45-55). At the time of the invention, it would have been obvious to one of ordinary skill in the art to continue the manufacturing of the integrated circuit of Singh by removing the first insulating film and forming gate oxide layers in between the first and second trenches because, as is taught by Ishitsuka, in this way, a transistor can be formed on the substrate.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,518,146) in view of Ishitsuka et al. (US 6,403,446) as applied to claim 6 above, and further in view of the admitted prior art.

Regarding claim 9, Singh discloses that the second element is a memory cell of a non-volatile memory and Singh discloses that the first element is a transistor, but Singh does not specifically state that the first element transistor is a MOS transistor. The admitted prior art discloses that the conventional transistor in the logic (peripheral) portion of this type of circuit is a MOS transistor (pg. 4, ln. 5-22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the logic (peripheral) transistor of Singh such that it is a MOS transistor because, as is taught by the admitted prior art, a MOS transistor is conventionally formed in the logic region of this type of integrated circuit.

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,518,146) in view of van Bentum et al. (US 20040119135).

Regarding claim 23, Singh discloses forming a first insulating film (20) in first and second regions of a semiconductor substrate (12), forming on the insulating film a second insulating film (18) made of a material different from that of the first insulating film, forming a first trench (14) by etching the first and second insulating films and the substrate in the second region, forming a second trench (16) by etching the first and second insulating films and the substrate in the first region, oxidizing the surfaces of the first and second trenches such that the curvature of an interface between a top edge portion of the first trench and the substrate is larger than the curvature of an interface between the top edge portion of the second trench and the substrate, forming a first element-isolating film and a second element-isolating film by filling the

first and second trenches with an insulating material (38) and removing the second insulating film (Fig. 1-5; col. 1, ln. 59 – col. 3, ln. 33). Singh discloses oxidizing the surfaces of both the first and second trenches at the same time. Singh does not disclose oxidizing the surface of the first trench and then oxidizing the surface of the second trench while further oxidizing the first trench. Like Singh, van Bentum discloses a method of creating two shallow trench isolation structures, one of which has a greater curvature of an interface between a top edge portion of the trench and the substrate. Van Bentum teaches that the trench that is to have the greater curvature can have its corners rounded by oxidizing the surface of that trench in a first step and then in a second step, oxidizing the surfaces of both the first trench and the second trench, so that the first trench is subjected to oxidation twice. In this manner, the upper corners of the first trench have a greater degree of rounding (curvature) than the second trench. At the time of the invention, it would have been obvious to one of ordinary skill in the art to oxidize the first trench of Singh and then oxidize both the first and second trenches because Singh states that the first trench should have greater corner-rounding than the second trench and van Bentum teaches that by subjecting the first trench to two oxidation steps, greater trench corner-rounding can be achieved.

Regarding claim 24, Singh discloses that the first insulating film is a pad oxide film and the second insulating film is a nitride film. But Singh does not specifically disclose that the first insulating film is a silicon oxide film nor that the second insulating film is a silicon nitride film. Van Bentum discloses that successful shallow trench isolation can be performed by using a pad silicon oxide film with a film of silicon nitride on top. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the pad oxide of Singh of silicon oxide and the nitride film of Singh of silicon nitride because van Bentum teaches that these

materials may successfully be used to accomplish the formation of a shallow trench isolation element.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,518,146) in view of van Bentum et al. (US 20040119135) as applied to claim 23 above, and further in view of the admitted prior art.

Regarding claim 25, Singh discloses that the second element is a memory cell of a non-volatile memory and Singh discloses that the first element is a transistor, but Singh does not specifically state that the first element transistor is a MOS transistor. The admitted prior art discloses that the conventional transistor in the logic (peripheral) portion of this type of circuit is a MOS transistor (pg. 4, ln. 5-22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the logic (peripheral) transistor of Singh such that it is a MOS transistor because, as is taught by the admitted prior art, a MOS transistor is conventionally formed in the logic region of this type of integrated circuit.

Allowable Subject Matter

Claims 13-22 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reasons for the allowance of claims 13-15 is the inclusion therein, in combination as currently claimed, of the limitations of forming two different shallow isolation trenches, one of which is formed by the etching the substrate such that the width of the trench is smaller than the width of the mask opening, while the other trench is formed by etching the substrate such that the width of the trench is equal to the width of the mask opening. These

limitations were found in claims 13-15 and are neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reasons for the allowance of claims 16-19 is the inclusion therein, in combination as currently claimed, of the limitations of forming two different shallow isolation trenches, one of which is etched into the substrate using a mask having a thick layer of insulating material, while the other trench is formed by etching the substrate using a mask having a thinner layer of the insulating material. These limitations were found in claims 16-19 and are neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reasons for the allowance of claims 20-22 is the inclusion therein, in combination as currently claimed, of the limitations of forming a first shallow isolation trench by forming a gap between an edge of the trench and an insulating film by performing heat treatment in a hydrogen atmosphere and forming a second shallow isolation trench. These limitations were found in claims 20-22 and are neither disclosed nor taught by the prior art of record, alone or in combination.

Claims 10-12 would be allowable if amended to overcome the objection to claim 10.

The primary reason for the indication of the allowable subject matter of claims 10-12 is the inclusion therein, in combination as currently claimed, of the limitation of forming two different shallow isolation trenches, one of which is etched into the substrate using a mask having a thick layer of insulating material, while the other trench is formed by etching the substrate using a mask having a thinner layer of the insulating material. This limitation is found in claims 10-12 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Yoo et al. (US 5,858,830) discloses forming a shallow trench isolation in a peripheral circuit region of a substrate and forming isolation regions having a greater curvature of its top corners in a memory circuit region of the substrate.

Shimizu (US 6,580,117) discloses forming a shallow trench isolation in a memory cell circuit region of a substrate such that it has rounded top corners while an isolation element is formed in the peripheral region of the substrate using "well-known techniques".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
July 6, 2004

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